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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/617,737	07/14/2003	Takashi Ohsawa	002372.00045	3632

22907 7590 09/07/2004

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EXAMINER	
WILSON, ALLAN R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/617,737	OHSAWA, TAKASHI	
	Examiner	Art Unit	
	Allan R. Wilson	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☒ Claim(s) *6-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/964,851.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/14/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 2 is objected to because of the following informalities: Fails to further limit claim 1. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5 are rejected under 35 USC § 102(b) as being anticipated by Hayashi et al. ("Hayashi") U.S. Patent No. 5,506,436.

With regards to claims 1-3, Hayashi illustrates in figures 1-18, particularly figures 10 and 11, (entire document) a semiconductor layer formed on the insulating film;

a source region L_2 formed in the semiconductor layer;

a drain region L_1 formed apart from the source region in the semiconductor layer, the semiconductor layer between the source region and the drain region serving as a channel body Ch_1 in a floating state;

a main gate G_2 formed on a first side of the channel body to form a channel in the channel body; and

an auxiliary gate G_1 formed on a second side of the channel body, the second side being opposite to the first side, a portion of the second side of the channel body being capable of accumulating majority carriers under conditions in which the channel body is fully depleted by an electric field from the main gate and an electric field is applied to the channel body from the auxiliary gate,

wherein the MISFET has a first data state in which the majority carriers are accumulated in the portion of the second side of the channel body and a second data state in which the majority carriers accumulated in the portion of the second side of the channel body are emitted,

wherein the MISFETS are arranged in the form of a matrix to constitute a cell array, the drain regions are connected to bit lines, the main gates constitute word lines intersecting the bit lines (2ND LINE), the source regions are connected to a fixed potential line (PREDETERMINED POTENTIAL) and the auxiliary gate is formed as a common electrode (1ST LINE) shared among the memory cells.

With regards to claim 1, the limitation "capable of accumulating majority carriers under conditions in which the channel body is fully depleted by an electric field from the main gate and an electric field is applied to the channel body from the auxiliary gate, wherein the MISFET has a first data state in which the majority carriers are accumulated in the portion of the second side of the channel body and a second data state in which the majority carriers accumulated in the portion of the second side of the channel body are emitted" is an inherent function of the structure and since the prior art has the same structure and materials as the claimed invention it will have the same inherent function.

With regards to claim 3, the examiner had to assume what the product would be by the process claimed. For example, in claim 3 it was assumed that the product was . The claim that it was "impact ionization" was not considered to have full patentable weight. A "product by process" claim is directed to the product per se, no matter how actually made, MPEP 2113 "Product-by-Process Claims," In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90; In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear.

With regards to claim 4, Hayashi illustrates in fig. 11 the first side of the channel body Ch_1 is a top side face of the semiconductor layer, the second side of the channel body is a back side face of the semiconductor layer and the main gate G_2 is formed on the top side face via a gate insulating film.

With regards to claim 5, Hayashi illustrates in fig. 11 the auxiliary gate G_1 is an impurity diffusion layer formed on the semiconductor substrate.

Allowable Subject Matter

Claims 6-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Yamazaki et al. (illustrates TFT with back gate electrodes) and Hanafi et al. (illustrates a double-gate MOSFET).

Field of Search	Date
U.S. Class and subclass: 257/365, 366	2 September 2004
Other Documentation: None	N/A
Electronic data base(s): EAST (USPAT, US-PGPUB, JPO, EPO, Derwent, IBM TDB)	2 September 2004

Any inquiry concerning this communication or earlier communications from an examiner should be directed to Primary Examiner Allan Wilson whose telephone number is (571) 272-1738. Examiner Wilson can normally be reached 7:00-4:00 Monday-Thursday and 6:00-3:00 on Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Allan R. Wilson
Primary Examiner
2 September 2004